|  |  |
| --- | --- |
| **Digital Logic Design**  Spring 2011 Semester  **Sessional-I**  Saturday, February 19, 2011  **Total Time: 60 Minutes**  **Total Marks: 35**  **Course Instructors:**  Mr. Raza-ur-Raheem, Mr. Mati Ullah Khan | Serial No:  Name \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  Section \_\_\_\_\_\_ Roll No: \_\_\_\_\_\_\_\_\_\_\_\_  Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  Signature of Invigilator |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q** | **1** | **2** | **3** | **Total** |
| **Total**  **Marks** | 10 | 10 | 15 | 35 |
| **Marks**  **Obtained** |  |  |  |  |

**You are advised to READ these notes:**

1. **Attempt on the Question Paper. NO EXTRA SHEET will be provided/accepted. No additional sheet will be provided for rough work. Use the back of the page where provided space is not sufficient.**
2. After asked to commence the exam, please verify that you have **different printed pages** including this title page.
3. There are **3 questions**. Attempt all of them. It is advisable to go through the paper once before starting with the first question.
4. Exam is closed books, closed notes. Please see that the area in your threshold is clean. You will be charged for any material which can be classified as ‘helping in the paper’ found near you.
5. **Calculator are not allowed.**
6. Students who attempt the paper with lead pencils loose the right to get them rechecked.
7. **The invigilator present is not supposed to answer any questions. No one may come to your room for corrections and you are not supposed to request to call anyone. Make assumptions wherever required and clearly mark them.**

**Question # 1[10]**

Design a combinational circuit that converts a four-bit Gray code to four bit binary information.

1. Write four-it Gray code as input and four-bit binary number as the output.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | W | X | Y | Z |
| 1 |  |  |  |  |  |  |  |
| 2 |  |  |  |  |  |  |  |
| 3 |  |  |  |  |  |  |  |
| 4 |  |  |  |  |  |  |  |
| 5 |  |  |  |  |  |  |  |
| 6 |  |  |  |  |  |  |  |
| 7 |  |  |  |  |  |  |  |
| 8 |  |  |  |  |  |  |  |
| 9 |  |  |  |  |  |  |  |
| 10 |  |  |  |  |  |  |  |
| 11 |  |  |  |  |  |  |  |
| 12 |  |  |  |  |  |  |  |
| 13 |  |  |  |  |  |  |  |
| 14 |  |  |  |  |  |  |  |
| 15 |  |  |  |  |  |  |  |
| 16 |  |  |  |  |  |  |  |

1. Write the function(82)10 = ( )6
2. (51.625) 10 = ( )2
3. (9AF)16 = ( )8
4. Convert the decimal numbers to binary 2’s complement form and perform subtraction:

(-9) – (-15)

**Question # 2[10]**

1. Convert given expression to standard SOP and POS

(AB + C)(D’)(ABD+A’B’)

1. Find the complement of F= x ( y'z' + yz )
2. Express the given function as sum of minterms and product of maxterms

F(A,B,C,D) = BC’ + AB + ACD

**Question # 3[15]**

1. Minimize the function: f(a,b,c,d) with minterms (1,3,4,5,9,11,12,13,14,15). Show k-map, and label ”essential prime implicants”.
2. Minimize the function f(a,b,c,d)with minterms (1,2,3,5,7) and Don’t Care conditions (10,11,12,13,14,15). Give k-map and Minimized SOP expression.
3. Simplify the following using k-map F(A,B,C) = A’B’ + AC’ + B’C + A’BC’
4. Simplify the expression:

F(w,x,y,z) = w’x’yz + w’xyz’ + wx’y’z + wxy’z’

and draw the circuit using

1. NAND gates
2. NOR gates